Low Threshold FETs for Low Power Cryogenic Electronics

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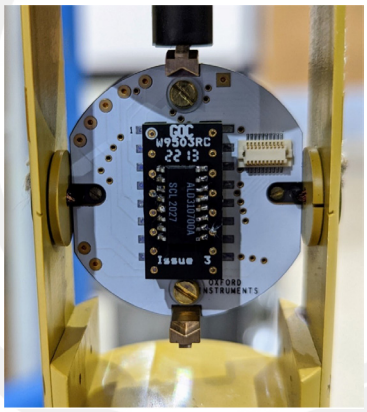
Introduction

In this Applications note, we demonstrate the low temperature characterisation of three low-threshold FETs (Field-Effect-Transistor) [1-3]. This allowed us to determine the key characteristics for cryogenic circuit design, such as threshold voltage, subthreshold slope and transconductance. The system used to cool these devices was the Oxford Instruments NanoScience **Teslatron**PT.

Motivation

Modern low-temperature research relies heavily upon cryogenic electronics and the most widely used device is the amplifier. Cryogenic amplifiers can be located close to a measurement to boost small signals, minimising the effects of noise further along the measurement chain and therefore increasing the signal-to-noise ratio. The bandwidth of a measurement can also be increased by impedance matching the amplifier output to the rest of the measurement chain. This enables smaller signals to be measured over a wider frequency range than would usually be possible in a passive system, increasing the amount of rich physics measurable in a cryogenic environment.

TeslatronPT



Zero Threshold p-Type FET mounted via a DIP converter.

The main limitation for cryogenic electronics is power dissipation. Excessive power dissipation at low temperatures can disrupt the temperature stability of the cryostat, increase the cooling power requirements and degrade sample measurement. Hence, it is of interest to identify FETs that can be incorporated into low power amplifiers optimised for use at cryogenic temperatures. Commercially available low-threshold FETs are good candidates, allowing the construction of circuitry requiring only very low supply voltages, minimising power dissipation.

Methods

In this experiment we mounted the FETs on a 16-pin DIP (Dual-Inline-Package) sample holder and inserted them into the **Teslatron**PT cryostat's MeasureProbe sample mount. The PCB is manufactured from Aluminium Nitride, a high thermal conductivity ceramic, to improve thermalisation.

Three low-threshold voltage FETs were measured. These consisted of a p-type and a n-type zero-threshold voltage FET and a n-type -0.4 V-threshold FET. The Drain-Source Current (I_{DS}) was taken as a function of the Drain-Source Voltage (V_{DS}) and then Gate-Source Voltage (V_{GS}). Figure 1 demonstrates the electrical circuit used. These I-V curves are taken using two Keithley 2450 SMUs in two-terminal mode at twenty different temperatures between 295 K and 1.5 K, evenly spaced on a logarithmic scale. Temperature control and stabilisation was provided by a **Mercury**iTC. The wiring resistance was recorded at each of these steps in a separate measurement, allowing us to subtract the effect of the wiring resistance from the I-V curves.

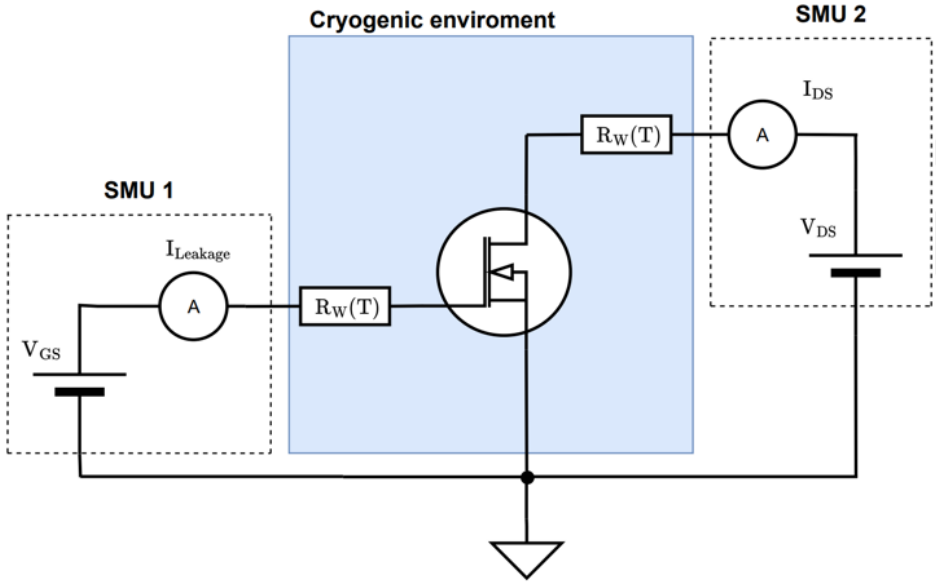


Figure 1: Electrical circuit of the measurement. Here $R_W(T)$ denotes the added effect of the temperature dependent wiring resistance in the two terminal measurement mode. IDS was measured as a function of both V_{GS} and V_{DS} to determine the FETs output characteristics as a function of temperature. $I_{Leakage}$ is the Gate leakage current, while this can be studied it wasn't part of our analysis.

Experimental Results

Figure 2 demonstrates the typical differences between low temperature and room temperature operation of the FETs. Figure 2a shows a sharpening of the subthreshold slope, a decrease in the off-state current and an increase in the threshold voltage. Figure 2b demonstrates the increase in transconductance at lower temperatures. These effects are well studied in the literature [4,5].

Figure 4 shows the threshold voltage as a function of temperature for all three FETs. Both n-type FETs (Figures 4a and 4c) demonstrate increasing thresholds that plateau at low temperature. The reason the p-type FET threshold does not plateau is not currently well described in the literature, but can be modelled by a temperature dependence on the gate oxide capacitance [4]. has a threshold of almost 0 V at low temperature, making it an ideal candidate for low voltage circuitry. The threshold voltage increase is attributed to both the increasing of

the silicon bandgap as well as the change in the Fermi potential of the (p-type doped) silicon substrate bulk [4]. Another notable feature of Figures 4a-c is the divergence of threshold values between V_{DS}= 1.5 V and V_{DS}= 50 mV at ~10 K that can likely be attributed to carrier freezeout. Further measurements in Figure 3 support this conclusion through the observation of the 'kink effect' in the zero threshold n-type FET, caused by impact ionisation in the FET channel. When electron-hole pairs are created by impact ionisation, the holes flow to the substrate bulk and the electrons flow to the drain, however due to dopant freezeout the bulk resistance has increased. The large voltage drop that occurs across the substrate bulk then lowers the threshold voltage of the FET via the body effect. This sudden decrease in the threshold voltage then corresponds to a sharp increase in Drain-Source current seen in Figure 3.

Both the zero threshold n-type and p-type FETs have non-zero thresholds at low temperatures, negating their use for low voltage applications. However, the depletion mode FET, which has a threshold of -0.4 V at room temperature has a threshold of almost 0 V at low temperature, making it an ideal candidate for low voltage circuitry.

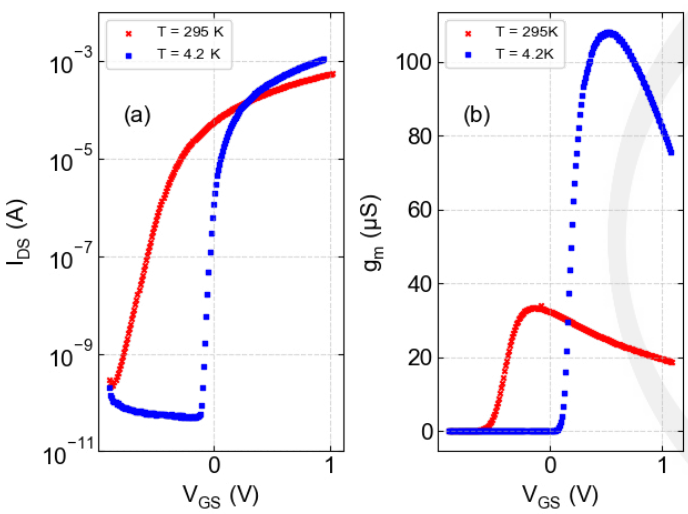


Figure 2: Characterisation of -0.4 V depletion mode FET a) Subthreshold regime. b) Transconductance at high drain bias.

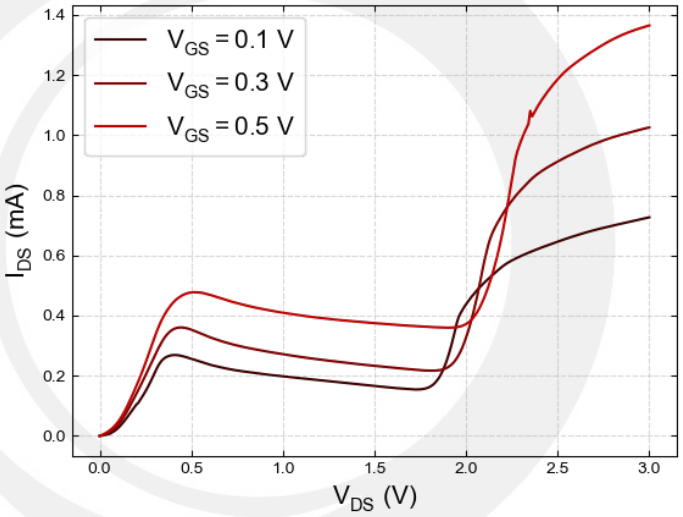


Figure 3: Impact Ionisation in a zero threshold n-type FET at 1.5 K. The shift of the kink is due to increased scattering of carriers in the channel reducing their mobility and requiring a larger drain voltage to cause impact ionisation.

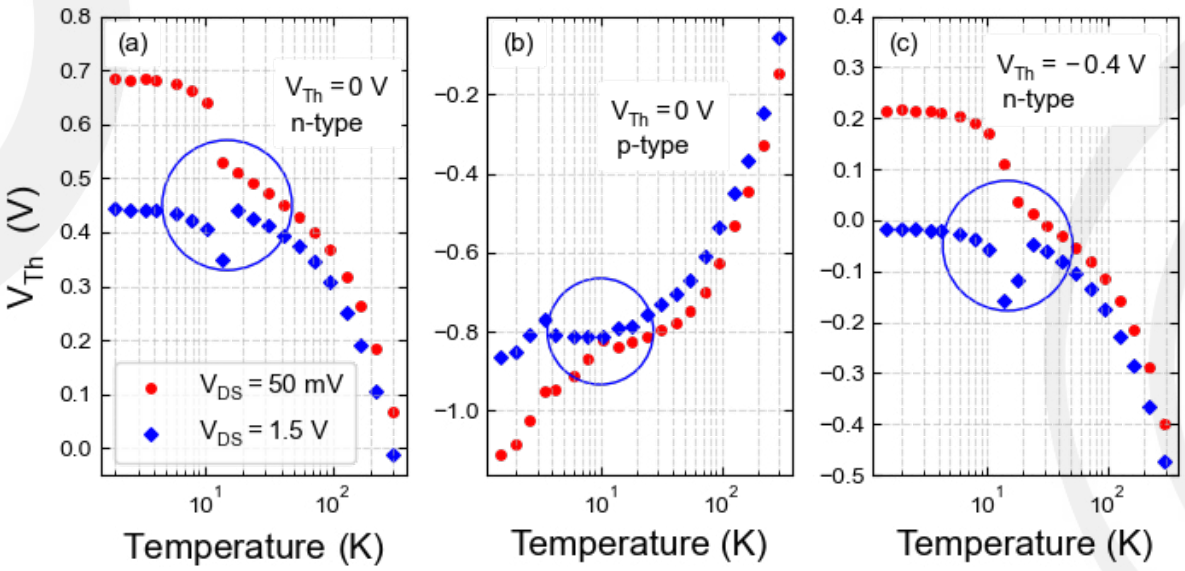


Figure 4: Threshold voltages as a function of temperature for three different low-threshold FETs. Here the blue circle indicates the onset of carrier freezeout at low temperature.

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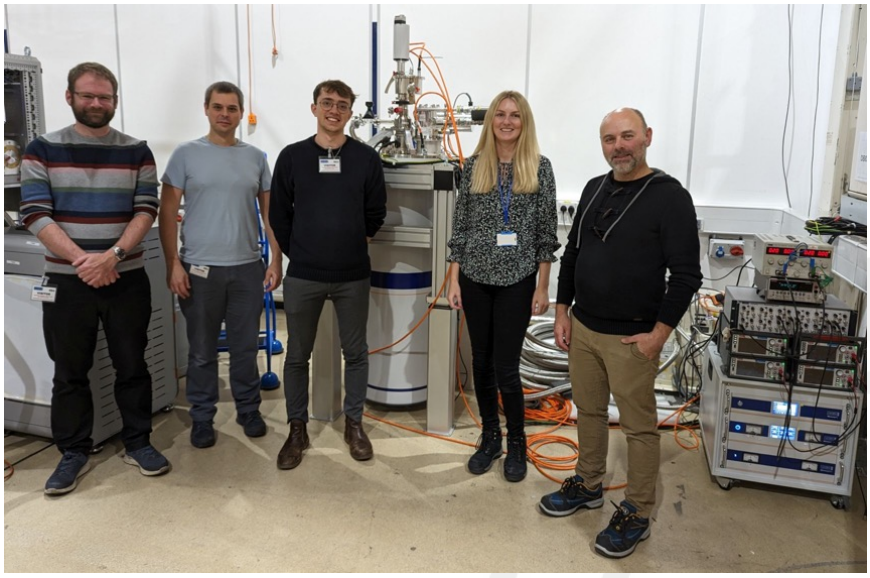
Conclusion

In this work we characterised three low threshold voltage FETs for potential use at cryogenic temperatures. We found that while all of the FETs exhibited large threshold increases it was possible to mitigate this increase by choosing FETs with negative room temperature thresholds. The specific devices chosen for this study were found to be unsuitable for cryogenic operation due to freezeout. This work, however, demonstrates the viability of utilising negatively-doped FETs in more modern, smaller, FET nodes which do not suffer from freezeout.

This could impact emerging fields of study such as cryo-CMOS for quantum computing, where this technique could be used to reduce the voltage supplies of cryo-electronics and therefore reduce power dissipation.

This work lead to the writing of a paper that quantifies the efficiency improvements in an amplifier when using FETs that have negative thresholds at room temperature. This paper is currently under review at the IEEE Journal of Electron Devices.



Left to right: Michael Thompson, Jonathan Prance, George Ridgard, Abigail Graham and Ben Yager

Citations

[1] ALD110800A, n-channel zero threshold MOSFET, https://www.aldinc.com/pdf/ALD110800.pdf
[2] ALD310700A, p-channel zero threshold MOSFET, https://www.aldinc.com/pdf/ALD310700.pdf
[3] ALD114804A, n-channel depletion mode MOSFET, https://www.aldinc.com/pdf/ALD114804.pdf
[4] Beckers, Arnout, et al. «Physical model of low-temperature to cryogenic threshold voltage in MOSFETs.» IEEE Journal of the Electron Devices Society 8 (2020): 780-788.
[5] Incandela, Rosario M., et al. «Characterization and compact modelling of manometer CMOS transistors at deep-cryogenic temperatures.» IEEE Journal of the Electron Devices Society 6 (2018): 996-1006.

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